



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of :

Venkatesh Gopinath
Arvind Kamath
Mohammad Mirabedini
Ming-Yi Lee

Serial No. : 09/991,202

Group Art Unit : 2812

Filed : November 14, 2001

Examiner : Isaac, Stanetta D.

For : Shallow Trench Isolation Structure
With Low Trench Parasitic
Capacitance

Atty Docket : / 01-555

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the date below:

Manu Kashyap

11-4-05
Date

Manu Kashyap
Signature

SUBMISSION OF FORMAL DRAWINGS PURSUANT TO 37 C.F.R. §1.85

Official Draftsman

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby substitutes the enclosed formal drawings for those presently in the above referenced application.

LSI Logic Corporation
1621 Barber Lane, MS D-106
Milipitas, CA 95035
408-433-7475

Date: 4 Nov 05

Respectfully submitted,

Timothy Croll

Reg. No. 36,771